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EXAMINER	
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ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 08/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/667,601	CHIDAMBARRAO ET AL.	
	Examiner	Art Unit	
	Jennifer M. Kennedy	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16,21,22,24 and 25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9, 13-16, 21-22, 24-25* is/are rejected.

7)☒ Claim(s) *10-12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 24 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. While the Applicants have support for forming the bird's beak is formed within the gate polysilicon and forms a stress within the channel region beneath the gate polysilicon. The Applicants have not provided support for "wherein the oxidizing step results in formation of a bird's beak in the channel of the gate polysilicon". The examiner notes that channel region of a transistor between the source and drain within the substrate and is beneath the polysilicon. Therefore, it is not clear how the bird's beak is formed in the channel of the gate polysilicon.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 24 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claim recites, "wherein the oxidizing step results in formation of a bird's beak in the channel of the gate polysilicon". The examiner notes that the Applicant has taught the bird's beak is formed within the gate polysilicon and forms a stress within the channel region beneath the gate polysilicon. The examiner notes that channel region of a transistor between the source and drain within the substrate and is beneath the polysilicon. Therefore, it is not clear how the bird's beak is formed in the channel of the gate polysilicon.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-2, 16, and 24-25 are rejected under 35 U.S.C. 102(e) as being anticipated by En et al. (U.S. Patent No. 6,573,172).

In re claim 1, En et al. disclose the method of forming an integrated circuit comprising a plurality of semiconductor devices including an n-type transistor (102) and a p-type transistor (104) on a semiconductor wafer, the method comprising:

covering the p-type transistor with a mask (130, 134); and

removing, after the oxidizing step, oxide above the gate polysilicon of the n-type transistor (see Figure 2I, in which the oxide 140 is removed to make contact to gate, and column 7, line 60 through column 8, line);

oxidizing a portion of a gate polysilicon of the n-type transistor, such that tensile mechanical stresses are formed within a channel of the n-type transistor (see column 6, line 65 through column 7, line 22).

Further, En et al. disclose the method wherein the oxide layer 140 is formed by thermal oxidation, which would necessarily result in formation of a bird's beak in an edge of the gate polysilicon as explained in Applicant's specification, page 10, lines 12-16).

In re claim 2, En et al. disclose the method wherein the step of covering comprises covering the p-type transistor with a mask made of nitride (130).

In re claim 16, En et al. teach the method of forming an integrated circuit comprising a plurality of semiconductor devices including an n-type transistor (102) and a p-type transistor (104) on a semiconductor wafer, the method comprising:

oxidizing a portion of a gate polysilicon of the n-type field effect transistor, such tat tensile mechanical stresses are formed within a channel of the n-type field effect transistor, without creating additional tensile stresses in a channel of the p-type transistor (see column 6, line 65 through column 7, line 22) and removing oxide above

the gate polysilicon of the n-type transistor (see Figure 2I, in which the oxide 140 is removed to make contact to gate, and column 7, line 60 through column 8, line);

Further, En et al. disclose the method wherein the oxide layer 140 is formed by thermal oxidation, which would necessarily result in formation of a bird's beak in an edge of the gate polysilicon as explained in Applicant's specification, page 10, lines 12-16).

In re claim 24, En et al. teach the method of forming an integrated circuit comprising a plurality of semiconductor devices including an n-type transistor (102) and a p-type transistor (104) on a semiconductor wafer, the method comprising:

oxidizing a portion of a gate polysilicon of the n-type field effect transistor, such tat tensile mechanical stresses are formed within a channel of the n-type field effect transistor, without creating additional tensile stresses in a channel of the p-type transistor (see column 6, line 65 through column 7, line 22).

Further, En et al. disclose the method wherein the oxide layer 140 is formed by thermal oxidation, which would necessarily result in formation of a bird's beak in an edge of the gate polysilicon as explained in Applicant's specification, page 10, lines 12-16).

In re claim 1, En et al. disclose the method of forming an integrated circuit comprising a plurality of semiconductor devices including an n-type transistor (102) and a p-type transistor (104) on a semiconductor wafer, the method comprising:

masking the p-type transistor (130, 134); and

depositing oxide on the gate polysilicon layer of the n-type transistor (see column 6, line 65 through column 7, line 22, En et al. teach depositing and a thermal method);

oxidizing a portion of a gate polysilicon of the n-type transistor, such that tensile mechanical stresses are formed within a channel of the n-type transistor (see column 6, line 65 through column 7, line 22, En et al. teach a deposition and a thermal method); and

removing oxide above the gate polysilicon of the n-type transistor (see Figure 2I, in which the oxide 140 is removed to make contact to gate, and column 7, line 60 through column 8, line);

Further, En et al. disclose the method wherein the oxide layer 140 is formed by thermal oxidation, which would necessarily result in formation of a bird's beak in the channel of the gate polysilicon as explained in Applicant's specification, page 10, lines 12-16).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

Claims 1, 6-9, 13-16, 21- 22, and 24-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bai et al. (U.S. Patent No. 6,204,103) in view of En et al. (U.S. Patent No. 6,573,172).

In re claims 1, 16, and 24, Bai et al. disclose the method for forming an integrated circuit comprising a plurality of semiconductor devices including an n-type transistor and a p-type transistor on a semiconductor wafer. Bai et al. does not disclose the method of covering the p-type transistor with a mask, depositing oxide on the gate polysilicon of the n-type transistor, and oxidizing a portion of a gate polysilicon of the n-type transistor, such that tensile mechanical stresses are formed within a channel of the n-type transistor without creating additional tensile stresses in a channel of the p-type transistor, removing, after the oxidizing step, oxide above the gate polysilicon of the n-type transistor, and wherein the oxidizing step results in formation of a bird's beak in an edge of the gate polysilicon.

En et al. disclose the method of covering the p-type transistor with a mask (130, 134); depositing oxide on the gate polysilicon of the n-type transistor, oxidizing a portion of a gate polysilicon of the n-type transistor, such that tensile mechanical stresses are formed within a channel of the n-type transistor (see column 6, line 65 through column 7, line 22) and removing, after the oxidizing step, oxide above the gate polysilicon of the n-type transistor (see Figure 2I, in which the oxide 140 is removed to make contact to gate, and column 7, line 60 through column 8, line).

Further, En et al. disclose the method wherein the oxide layer 140 is formed by thermal oxidation, which would necessarily result in formation of a bird's beak in an edge of the gate polysilicon as explained in Applicant's specification, page 10, lines 12-16).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to cover the p-type transistor with a mask and oxidize the gate polysilicon of the n-type transistor, such that tensile mechanical stresses are formed within a channel of the n-type transistor without creating additional tensile stresses in a channel of the p-type transistor because as En et al. teach increasing the tensile stresses in the NMOS region while preventing the increasing of the tensile stresses in the PMOS region increases carrier mobility (see column 2, lines 11-28).

Further, it would have been obvious to one of ordinary skill in the art at the time the invention was made to remove, after the oxidizing step, oxide above the gate polysilicon of the n-type transistor in order to allow for electrical interconnection to the top of the gate.

In re claim 6, Bai et al. disclose the method of forming a planarized oxide layer on the semiconductor wafer (1516).

In re claim 7 and 8, Bai et al. disclose the method comprising removing silicide (1505) material from above the gate polysilicon of the n-type field effect transistor, and wherein the step of removing silicide material form above the gate polysilicon of the n-type field effect transistor comprises etching the silicide material form above the gate polysilicon of the n-type field effect transistor (see column 6, lines 50-62).

In re claim 9, En et al. disclose the method wherein the removing step comprises removing deposited oxide (140) from above the gate polysilicon of the n-type field effect transistor by etching the deposited oxide from above the gate polysilicon of the n-type

field effect transistor (see Figure 2I, in which the oxide 140 is removed to make contact to gate, and column 7, line 60 through column 8, line).

In re claim 13, Bai et al. disclose the method of depositing at least one of a silicide material or a nitride cap on at least the gate polysilicon of the n-type field effect transistor and removing silicide material or the nitride cap form above the gate polysilicon of the no-type field effect transistor prior to performing the step of oxidizing (see column 6, lines 50-63).

In re claims 14 and 15, En et al. does not disclose the range of tensile stress created in the n-type FET. En et al. however, does disclose the method of oxidizing the polysilicon gate by the same method of Applicants, and it would be expected that the same range of tensile stress would be created by the oxidation step. However, the examiner notes that Applicant does not teach that the tensile stress range solve any stated problem or are for any particular purpose. Therefore, the tensile stress range lacks criticality in the claimed invention and does not produce unexpected or novel results. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the NFET with a tensile stress range as claimed, since the invention would perform equally well as long as sufficient tensile stress is applied to the NMOS region to increase the carrier mobility, as En et al. teach, and because it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233, MPEP 2144.05 II A.

In re claim 21, the combined Bai et al. and En et al. disclose the method wherein the step of oxidizing a portion of a gate polysilicon of the n-type transistor is performed after silicidation of the gate polysilicon. En et al. teach that the oxidation can be made after the silicidation (108) of the NMOS (see column 6, lines 12-21).

In re claim 22, the combined Bai et al. and En et al. disclose the method wherein the tensile stresses are formed along a longitudinal direction of the channel of the n-type transistor. The examiner notes that the longitudinal direction is arbitrary. The examiner maintains that En et al. disclose the stresses are created in the channel, and thus are formed along a longitudinal direction of the channel of the n-type transistor.

In re claim 25, the combined Bai et al. and En et al. disclose the method wherein the removing step preserves the bird's beak (see Figure 2I, in which the oxide 140 is removed to make contact to gate, and column 7, line 60 through column 8, line). THe examiner notes since the bird's beaks are formed on the edge of the polysilicon and the interconnection is formed only in the central region of the gate then the removing step would preserve the bird's beak.

Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over En et al. (U.S. Patent No. 6,573,172) in view of Chang (U.S. Patent No. 6,461,981).

En et al. disclose the method as claimed including the method of forming the oxide by a thermal oxide method, but does not disclose the particular conditions of the oxidation, and therefore the particular conditions used to form the oxide layer lacks criticality in the invention of En et al. One of ordinary skill in the art at the time the

invention was made would have recognized that any known method and conditions could be used to form the oxide layer, in the absence of a particular suggestion by En et al.

Chang discloses the method of a conventional oxidation of polysilicon wherein oxidation is performed by using low temperature oxidation, wherein the oxidation is performed about 25 degrees C to about 600 degrees C, and wherein the oxidation is at least one of high pressure oxidation, or atomic oxidation or plasma oxidation (see column 3, lines 25-40). It would have been obvious to one of ordinary skill in the art at the time the invention was made to thermal oxidize the polysilicon by the method of Chang since the conditions of forming the oxide layer lacks criticality in the invention of En et al. and since the method of Chang is a known method of forming an oxide with conditions are effective to oxidize the polysilicon to form an oxide layer.

Response to Arguments

Applicant's arguments with respect to claim May 20, 2005 have been considered but are not persausive.

Applicants argue, on Page 7 of the response, "a prima facie case of anticipation cannot be established because SAUNDERS fails to teach each and every element of the claims." The examiner notes that she has not relied upon SAUNDERS for rejection.

Applicants argue that En et al. do not disclose the method of removing the oxide above the gate polysilicon referring the examiner to column 7, lines 36-39. The examiner notes that En et al. does disclose removing oxide above the gate polysilicon

of the n-type transistor (see Figure 2I, in which the oxide 140 is removed to make contact to gate, and column 7, line 60 through column 8, line).

Applicants also argue that En et al. does not have a bird's beak region. En et al. disclose the method wherein the oxide layer 140 is formed by thermal oxidation, which would necessarily result in formation of a bird's beak in the channel of the gate polysilicon as explained in Applicant's specification, page 10, lines 12-16).

Further, Applicants argue that the bird's beak is not arranged within the channel of the n-type field effect transistor. The examiner notes that the Applicant has taught the bird's beak is formed within the gate polysilicon and forms a stress within the channel region beneath the gate polysilicon. The examiner notes that channel region of a transistor between the source and drain within the substrate and is beneath the polysilicon. Therefore, it is not clear how in Applicants method the bird's beak is formed in the channel of the gate polysilicon.

Applicants again argue that the claimed range of stress is critical, citing passages within the specification. The Applicants point the examiner to Figures 4 and 5 where there are examples of 700 MPa are shown, and to page 2 of the specification wherein the conventional tensile stresses are moderate at (200MPa to 300 MPa). The Applicants then point the examiner to Page 10 in which the Applicants state

> the oxidation of the gate of the NFETS creates large tensile stresses in the channel region of the NFETS ... Further, these tensile stresses increase electron mobility along the channel, and improve the performance of the NFETS.

However, the examiner notes that En et al. also oxidizes the gate of the NFET, and thus, this recitation only supports that En et al. method would necessarily result in the same tensile stresses as Applicant's method and the formation of a bird's beak in the channel of the gate polysilicon.

The examiner still maintains that nowhere in the specification is the range of 500Pa to 1000Pa or 700MPa cited as a critical range. The examiner notes that while many passages discuss the advantage of increased tensile stress, the passages do not state the criticality of the range. Further, on page 13, applicants state that "the **desired** stresses are tensile and add values **of the order of 200MPa** and above." First, the examiner notes again, that the claimed range is desired, not critical. Further, the examiner notes that applicant is teaching in this passage that 200MPa is sufficient and therefore the range of 500 to 1000Pa or 700MPa is not critical. Also, the examiner notes that the language of "of the order" suggests that the order of magnitude desired is within the hundreds. Finally, the examiner notes that Applicant's admit on page 2 of the specification that known methods are able to provide 200 to about 300 MPa of tensile stress.

Please note that the range claimed in Claim 15 of 500 Pa to 1000 Pa is less than that of 200 to 300 MPa that is taught to be conventional by Applicants.

While Applicants have pointed to examples having 700 MPa and conventional amounts of strain, this does not negate the fact that Applicants have also taught "the **desired** stresses are tensile and add values **of the order of 200MPa** and above." This

statement clearly teaches that the claimed range of 500 to 1000 Pa or 700 MPa is not critical.

The other arguments, with respect to the 103 rejections with Bai et al. and Chang et al. presented by Applicants rely on the alleged deficiencies of En et al. that are discussed above.

Allowable Subject Matter

Claims 10-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: the prior art, either singly or in combination, fails to anticipate or render obvious, the method including the limitations of oxidizing a p9ortion of a gate polysilicon of the n-type transistor, such that tensile mechanical stresses are formed within a channel of the n-type transistor, wherein the oxidizing step results in formation of a bird's beak in an edge of the gate polysilicon and removing, after the oxidizing step, oxide above the gate polysilicon of the n-type transistor, wherein the removing step comprises removing a deposited oxide from above the gate polysilicon of the n-type field effect transistor by etching the deposited oxide from above the gate polysilicon of the n-type field effect transistor and comprising depositing silicide material on at least the portion of the gate polysilicon of the n-type field effect transistor.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Ueno et al. (U.S. Patent Appl. 2004/0046219) disclose the diffusion mechanism of oxygen during a thermal oxidation to create bird's beak. Ishihara et al. (U.S. Patent No. 4,465,705) disclose that bird's beak formation is inherent in oxidation processes (see column 2, lines 55-68).

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Kennedy whose telephone number is (571) 272-1672. The examiner can normally be reached on Mon.-Fri. 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Kennedy
Primary Examiner
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jmk